REMARKS

Initially, Applicants filed an Information Disclosure Statement (IDS) on January 19, 2005. The Examiner has not acknowledged receipt of this IDS. Applicants provide herewith a copy of the IDS, including the stamped postcard. Applicants respectfully request that the Examiner consider the documents cited in connection with the IDS by initialing and returning a copy of the Form 1449 that accompanies the IDS.

In the final Office Action, the Examiner rejected claims 1, 4-6, 9-12, 15-17, 19, and 22-24 under 35 U.S.C. § 102(e) as anticipated by Roy et al. (U.S. Patent No. 6,646,983); and rejected claims 2, 3, 8, 14, 20, 21, and 25-27 under 35 U.S.C. § 103(a) as unpatentable over Roy et al. in view of Ben-Zur et al. (U.S. Patent No. 6,754,174). The Examiner objected to claims 7, 13, and 18 as dependent upon a rejected base claim, but indicated that these claims would be allowable if rewritten into independent form to include the features of the base claim and any intervening claims.

Applicants appreciate the Examiner's indication of allowable subject matter, but respectfully traverse the Examiner's rejections under 35 U.S.C. §§ 102 and 103. Claims 1-27 remain pending.

IMPROPER FINAL REJECTION

At the outset, Applicants respectfully submit that the finality of the Office Action, dated September 20, 2005, is improper. In the previous Office Action, dated February 23, 2005, the Examiner rejected dependent claims 9 and 15 under 35 U.S.C. § 103(a) as unpatentable over Roy et al. and Ben-Zur et al. Claims 9 and 15 recite that certain components are integrated onto a single chip. In the February 23, 2005 Office Action, the Examiner admitted that Roy et al. does

not disclose the features of claims 9 and 15.

Applicants subsequently filed an Amendment on May 20, 2005 with no change to claim 9 or 15. In the final Office Action, dated September 20, 2005, the Examiner newly rejected dependent claims 9 and 15 under 35 U.S.C. § 102(e) as anticipated by Roy et al. The Examiner alleged that Roy et al. discloses the features of claims 9 and 15 and made the rejection final.

M.P.E.P. § 706.07(a) states that:

> second or any subsequent actions on the merits shall be final, except where the examiner introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims nor based on information submitted in an information disclosure statement filed during the period set forth in 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p).

Applicants amendment filed May 20, 2005 could not have necessitated the Examiner's application of a new ground of rejection with regard to claims 9 and 15. Further, the Roy et al. and Ben-Zur et al. references were not cited by Applicants in an Information Disclosure Statement filed during the period set forth in 37 CFR 1.97(c). Accordingly, Applicants submit that the finality of the Office Action, dated September 20, 2005, is improper. Withdrawal of the finality of the Office Action, dated September 20, 2005, is, therefore, respectfully requested.

REJECTION UNDER 35 U.S.C. § 102

In paragraph 2 of the Office Action, the Examiner rejected claims 1, 4-6, 9-12, 15-17, 19, and 22-24 under 35 U.S.C. § 102(e) as allegedly anticipated by Roy et al. Applicants respectfully traverse the rejection.

A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either expressly or impliedly. Any feature not directly taught must be inherently present. In other words, the identical invention must be shown in as complete

detail as contained in the claim. See M.P.E.P. § 2131. Roy et al. does not disclose or suggest the combination of features recited in claims 1, 4-6, 9-12, 15-17, 19, and 22-24.

Independent claim 1, for example, is directed to an apparatus for interfacing a high-speed link to a network device. The apparatus comprises a receiver module, a framer module, and a sprayer module. The receiver module operates at a first clock rate for receiving a stream of in-coming data from the high-speed link. The framer module operates at a second clock rate for deserializing the stream of in-coming data onto a multi-line bus and extracting data packets from the deserialized data on the multi-line bus, wherein the second clock rate is lower than the first clock rate. The sprayer module is configured to receive the extracted data packets from the framer module and, for each of the extracted data packets, select one of a plurality of processing paths in the network device and transmit the extracted data packet to the selected processing path.

Roy et al. does not disclose or suggest the combination of features recited in claim 1. For example, Roy et al. does not disclose or suggest a sprayer module that is configured to receive extracted data packets from a framer module and for each of the extracted data packets, select one of a plurality of processing paths in the network device and transmit the extracted data packet to the selected processing path.

The Examiner alleged that Roy et al. discloses a sprayer module (final Office Action, page 2). The Examiner identified elements 16, 18, 20, and 22, and column 11, lines 2-8, of Roy et al. as allegedly corresponding to the sprayer module and for the first time the Examiner also identified elements 26, 52, 72, and 80 and column 13, lines 6-10, of Roy et al. as allegedly

corresponding to the sprayer module (final Office Action, page 2). Applicants respectfully disagree.

Roy et al. identifies element 16 as a pointer processor, element 18 as a path overhead (POH) processor, element 20 as an HDLC framer, and element 22 as a cell delineation block (col. 10, line 35, - col. 11, line 39). Roy et al. discloses that pointer processor 16 uses a SONET pointer to correctly locate the start of payload data being carried in a SONET envelope (col. 10, lines 35-37). Nowhere does Roy et al. disclose or suggest that pointer processor 16 receives extracted data packets from a framer module and, for each of the extracted data packets, selects one of a plurality of processing paths in the network device and transmits the extracted data packet to the selected processing path, as required by claim 1.

Roy et al. discloses that POH processor 18 processes nine bytes of path overhead in each of forty-eight SONET SPEs (col. 10, lines 54-55). Nowhere does Roy et al. disclose or suggest that POH processor 18 receives extracted data packets from a framer module and, for each of the extracted data packets, selects one of a plurality of processing paths in the network device and transmits the extracted data packet to the selected processing path, as required by claim 1.

Roy et al. discloses that HDLC framer 20 performs HDLC framing and forwards a PPP packet to a FIFO buffer, where it awaits assembly into PDUs (col. 11, lines 18-20). Nowhere does Roy et al. disclose or suggest that HDLC framer 20 receives extracted data packets from a framer module and, for each of the extracted data packets, selects one of a plurality of processing paths in the network device and transmits the extracted data packet to the selected processing path, as required by claim 1.

Roy et al. discloses that cell delineation block 22 performs cell mapping as described in an ITU-T G.804 publication (col. 11, lines 29-31). Nowhere does Roy et al. disclose or suggest that cell delineation block 22 receives extracted data packets from a framer module and, for each of the extracted data packets, selects one of a plurality of processing paths in the network device and transmits the extracted data packet to the selected processing path, as required by claim 1.

As explained in Applicants' prior response, Roy et al. does not disclose that any of pointer processor 16, POH processor 18, HDLC framer 20, and/or cell delineation block 22 receives extracted data packets from a framer module and, for each of the extracted data packets, selects one of a plurality of processing paths in the network device and transmits the extracted data packet to the selected processing path, as required by claim 1. Therefore, even assuming, for the sake of argument, that it is reasonable to identify all of these elements as corresponding to the sprayer module recited in claim 1 (a point that Applicants do not concede), the sprayer module recited in claim 1 would not result.

The Examiner also identified column 11, lines 2-8, of Roy et al. as allegedly disclosing the sprayer module of claim 1 (Office Action, pages 2-3). Applicants respectfully disagree.

At column 10, line 66, through column 11, line 8, Roy et al. discloses:

> Once the frame boundaries of the incoming SONET/SDH signals are found and the location of the SPEs has been identified either through pointer processing or through Telecom bus I/F control signals, and the Path Overhead is processed, the payload is extracted from the SPE. The SPEs may be carrying TDM traffic, ATM cells or IP packets. The type of traffic for each SPE is configured through the microprocessor interface 78. Each SPE can carry only one type of traffic. The data from each SPE is routed directly to the correct payload extractor.

Contrary to the Examiner's allegation, nowhere in this section, or elsewhere, does Roy et al. disclose or suggest a sprayer module that is configured to receive extracted data packets from a framer module and for each of the extracted data packets, select one of a plurality of processing

paths in the network device and transmit the extracted data packet to the selected processing path, as required by claim 1.

In response to similar arguments by Applicants in a prior response, the Examiner alleged that elements 16, 18, 20, and 22 are the elements required to process and extract the data packets and elements 26, 52, 72, and 80 correspond to a "receive switch controller" that "functions and suggests to receive extracted data packets from a framer module and for each for the extracted data packets, select one of a plurality of processing paths in the network device and transmit the extracted data packet to the selected processing path" (final Office Action, page 9). Applicants respectfully disagree.

Initially, Roy et al. does not disclose that elements 26, 52, 72, and 80 correspond to a receive switch controller, as alleged by the Examiner. Instead, Roy et al. discloses that elements 52, 56, 72, and 80 are collectively referred to as a receive switch controller (col. 13, lines 6-10). Therefore, the Examiner's allegation that elements 26, 52, 72, and 80 operate together as a receive switch controller that is allegedly equivalent to the sprayer module recited in claim 1 lacks merit. Applicants respectfully submit that none of elements 26, 52, 56, 72, and 80, whether operating alone or in combination, can reasonably be equated to the sprayer module recited in claim 1.

Roy et al. identifies element 26 as a low order pointer processor, element 52 as a switch mapper, element 56 as a request arbiter, element 72 as a data link manager, and element 80 as a weighted round robin scheduler (col. 5, lines 19-64). Roy et al. discloses that low order pointer processor 26 receives time division multiplexed (TDM) data and identifies low order virtual tributary structures (VTs) and virtual containers (VCs) (col. 11, lines 40-42). Nowhere does Roy

et al. disclose or suggest that low order pointer processor 26 receives extracted data packets from a framer module and, for each of the extracted data packets, selects one of a plurality of processing paths in the network device and transmits the extracted data packet to the selected processing path, as required by claim 1.

Roy et al. discloses that switch mapper 52 receives TDM data and arranges the TDM data, protocol data units (PDUs), and request elements in a frame (col. 12, lines 55-64). Nowhere does Roy et al. disclose or suggest that switch mapper 52 receives extracted data packets from a framer module and, for each of the extracted data packets, selects one of a plurality of processing paths in the network device and transmits the extracted data packet to the selected processing path, as required by claim 1.

Roy et al. discloses that request arbiter 56 forms request elements from control headers and forwards the requests to switch mapper 52 for transmission through the switch (col. 13, lines 43-45). Nowhere does Roy et al. disclose or suggest that request arbiter 56 receives extracted data packets from a framer module and, for each of the extracted data packets, selects one of a plurality of processing paths in the network device and transmits the extracted data packet to the selected processing path, as required by claim 1.

Roy et al. discloses that data link manager 72 aggregates control headers required for transmission of cells through the switch into the QoS queues and inserts routing tags into one of thirty-one QoS routing tag FIFOs (col. 13, lines 29-32). Nowhere does Roy et al. disclose or suggest that data link manager 72 receives extracted data packets from a framer module and, for each of the extracted data packets, selects one of a plurality of processing paths in the network

device and transmits the extracted data packet to the selected processing path, as required by claim 1.

Roy et al. discloses that weighted round robin scheduler 80 uses a weighted round robin scheduling technique on the QoS queues to schedule cell containers for transmission (col. 13, lines 37-45). Nowhere does Roy et al. disclose or suggest that scheduler 80 receives extracted data packets from a framer module and, for each of the extracted data packets, selects one of a plurality of processing paths in the network device and transmits the extracted data packet to the selected processing path, as required by claim 1.

The Examiner also identified column 13, lines 6-10, of Roy et al. as allegedly disclosing the sprayer module of claim 1 (final Office Action, page 2). Applicants respectfully disagree.

At column 13, lines 6-10, Roy et al. discloses:

> In section 9 of Appendix A, the data link manager 72, arbiter block 56, switch mapper 52, and weighted round robin scheduler 80, together with memory and other support circuits (not shown in FIG. 1) are referred to collectively as the "receive switch controller".

Contrary to the Examiner's allegation, nowhere in this section, or elsewhere, does Roy et al. disclose or remotely suggest a sprayer module that is configured to receive extracted data packets from a framer module and for each of the extracted data packets, select one of a plurality of processing paths in the network device and transmit the extracted data packet to the selected processing path, as required by claim 1.

In addition, Applicants respectfully submit that it is wholly unreasonable to equate eight distinct elements of Roy et al. as allegedly corresponding to the sprayer module recited in claim 1. Nevertheless, as explained above, none of these elements, either alone or in any reasonable combination, is configured to receive extracted data packets from a framer module and for each

of the extracted data packets, select one of a plurality of processing paths in the network device and transmit the extracted data packet to the selected processing path, as required by claim 1.

For at least the foregoing reasons, Applicants submit that claim 1 is not anticipated by Roy et al. Claims 4-6 and 9-11 depend from claim 1 and are, therefore not anticipated by Roy et al. for at least the reasons given with regard to claim 1. Claims 4-6 and 9-11 are also not anticipated by Roy et al. for reasons of their own.

For example, claim 4 recites that the plurality of processing paths includes a plurality of preprocessing modules for processing the extracted data packets. Roy et al. does not disclose or suggest the combination of features recited in claim 4.

The Examiner did not address the features of claim 4. Therefore, the Examiner did not establish a proper case of anticipation with regard to claim 4. Applicants identified this deficiency in the Examiner's rejection in a prior response. The Examiner still did not address the features of claim 4. If the Examiner persists with the rejection of claim 4 as allegedly being anticipated by Roy et al., Applicants request that the Examiner specifically identify where the features of claim 4 are disclosed by Roy et al., or withdraw the rejection.

For at least these additional reasons, Applicants submit that claim 4 is not anticipated by Roy et al.

Claim 6 recites that the sprayer module is configured to transmit each extracted data packet to one of the plurality of preprocessing modules based on a load balancing technique. Roy et al. does not disclose or suggest the combination of features recited in claim 6.

The Examiner alleged that Roy et al. discloses these features and cited column 3, lines 8-24, column 17, lines 11-17, and column 23, claims 4 and 5, of Roy et al. for support (final Office Action, page 3). Applicants respectfully disagree.

At column 3, lines 7-24, Roy et al. discloses:

> A typical switch according to the invention includes multiple port processors and multiple switch elements. For a 48x48 "folded" switch, 48 port processors are coupled (four each) to 12 (first and third stage) switch elements and each of these twelve switch elements is coupled to 8 (second stage) switch elements. A three stage non-blocking switch according to the invention provides a total bandwidth of 240 Gbps and a five stage non-blocking switch provides a total bandwidth of 1 Tbps. An exemplary three stage folded Clos architecture switch includes forty-eight port processors and twenty switch elements. Four port processors are coupled to each of twelve (first and third stage) switch elements. Each of the twelve (first and third stage) switch elements are coupled to eight (second stage) switch elements. According to the presently preferred embodiment, each port processor is provided with means for coupling to two ports of a switch element or one port of two switch elements thereby providing redundancy in the event of a link failure.

Nowhere in this section does Roy et al. disclose or suggest that any of the elements that the Examiner alleged were equivalent to the sprayer module (i.e., elements 16, 18, 20, 22, 26, 52, 56, 72, and 80) transmits each extracted data packet to one of the plurality of preprocessing modules based on a load balancing technique, as required by claim 6. In fact, Roy et al. does not even mention load balancing.

At column 17, lines 11-17, Roy et al. discloses:

> [Data stream deserializer 126] recovers the thirty-six-bit slot data from the row stream in a third FIFO which is used for deskewing the twelve input links. This deskewing allows all the input links to forward slot N to the switching core simultaneously. The link deskewing is controlled by the link synchronization and timing control module 150.

Nowhere in this section does Roy et al. disclose or suggest that any of the elements that the Examiner alleged were equivalent to the sprayer module (i.e., elements 16, 18, 20, 22, 26, 52, 56, 72, and 80) transmits each extracted data packet to one of the plurality of preprocessing modules based on a load balancing technique, as required by claim 6.

In claims 4 and 5, Roy et al. discloses:

> 4. A communications switch comprising:
>
> a) a plurality of port processors, each having at least one network interface; and
>
> b) a plurality of switch elements, each having a plurality of ports for coupling to said port processors, wherein
>
> each of said port processors has first and second switch element interfaces for coupling to two ports of a single switch element, and
>
> each of said port processors has automatic means for redirecting traffic to either of said first or second switch element interfaces in the event of a switch failure or congestion.
>
> 5. A communications switch according to claim 4, wherein:
>
> each of said ports comprises two serial links which are interleaved to effectively double the bandwidth of a single serial link.

Nowhere in these claims does Roy et al. disclose or suggest that any of the elements that the Examiner alleged were equivalent to the sprayer module (i.e., elements 16, 18, 20, 22, 26, 52, 56, 72, and 80) transmits each extracted data packet to one of the plurality of preprocessing modules based on a load balancing technique, as required by claim 6.

For at least these additional reasons, Applicants submit that claim 6 is not anticipated by Roy et al.

Claim 9 recites that the receiver module, the framer module, the sprayer module, the plurality of preprocessing modules, and the plurality of memories are integrated onto a single chip. Roy et al. does not disclose or suggest the combination of features recited in claim 9.

The Examiner alleged that Roy et al. discloses the features of claim 9 and cited claim 6 of Roy et al. for support. Applicants have carefully studied claim 6 and submit that the features of claim 9 are not disclosed or remotely suggested therein. If the Examiner persists with this

rejection, Applicants respectfully request that the Examiner specifically identify what portion of claim 6 of Roy et al. allegedly corresponds to the features of claim 9.

For at least these additional reasons, Applicants submit that claim 9 is not anticipated by Roy et al.

Claim 11 recites a desprayer module for receiving data packets from the plurality of processing paths and transmitting the received data packets to the deframer module. Roy et al. does not disclose or suggest the combination of features recited in claim 11.

The Examiner alleged that Roy et al. discloses a desprayer module and identified elements 26, 28, 60, 140, and 142, column 15, lines 29-47, and column 19, lines 19-42, of Roy et al. for support (final Office Action, page 4). Applicants respectfully disagree.

Applicants have carefully studied each of the elements and sections identified by the Examiner and respectfully submit that none of them can reasonably be alleged to correspond to, or disclose, a desprayer module for receiving data packets from the plurality of processing paths and transmitting the received data packets to the deframer module, as required by claim 11. If the Examiner persists with this rejection, Applicants respectfully request that the Examiner explain how the above identified elements and sections can reasonably be interpreted to correspond to the features recited in claim 11.

For at least these additional reasons, Applicants submit that claim 11 is not anticipated by Roy et al.

Independent claim 12 is directed to an apparatus for interfacing at least one line interface card to a plurality of switching/forwarding modules of a network device. The apparatus comprises a plurality of preprocessing modules for processing data packets and transmitting the

processed data packets to respective switching/forwarding modules, and a sprayer module for receiving data packets from at least one line interface card and, for each received data packet, selecting one of the plurality of preprocessing modules and transmitting the received data packet to the selected preprocessing module.

Roy et al. does not disclose or suggest the combination of features recited in claim 12. For example, Roy et al. does not disclose or suggest a sprayer module for receiving data packets from at least one line interface card and, for each received data packet, selecting one of the plurality of preprocessing modules and transmitting the received data packet to the selected preprocessing module.

The Examiner alleged that Roy et al. discloses a sprayer module and identified elements 16, 18, 20, 22, 26, 52, 72, and 80, column 11, lines 2-8, and column 13, lines 6-10, of Roy et al. for support (final Office Action, page 4). Applicants respectfully disagree for reasons similar to reasons given with regard to claim 1.

For at least the foregoing reasons, Applicants submit that claim 12 is not anticipated by Roy et al. Claims 15 and 16 depend from claim 12 and are, therefore, not anticipated by Roy et al. for at least the reasons given with regard to claim 12. Claims 15 and 16 also recite features similar to, but different in scope from, features recited in claims 9 and 11. Claims 13 and 16 are, therefore, also not anticipated by Roy et al. for at least reasons similar to reasons given with regard to claims 9 and 11.

Independent claim 17 is directed to a networking device. The networking device comprises a sprayer module, a plurality of preprocessing modules, and a plurality of switching/forwarding modules. The sprayer module is for receiving data packets and, for each of

the data packets, selecting one of a plurality of channels and outputting the data packet on the selected channel. The plurality of preprocessing modules are for processing data packets. Each preprocessing module receives data packets from one of the channels of the sprayer module. Each switching/forwarding module receives data packets from a corresponding one of the plurality of preprocessing modules.

Roy et al. does not disclose or suggest the combination of features recited in claim 17. For example, Roy et al. does not disclose or suggest a sprayer module for receiving data packets and, for each of the data packets, selecting one of a plurality of channels and outputting the data packet on the selected channel.

The Examiner alleged that Roy et al. discloses a sprayer module and identified elements 16, 18, 20, 22, 26, 52, 72, and 80, column 11, lines 2-8, and column 13, lines 6-10, of Roy et al. for support (final Office Action, pages 4-5). Applicants respectfully disagree for reasons similar to reasons given with regard to claim 1.

Roy et al. also does not disclose or suggest a plurality of preprocessing modules for processing data packets, where each processing module receives data packets from one of the channels of the sprayer module, as further recited in claim 17. The Examiner alleged that Roy et al. discloses a plurality of preprocessing modules and identified elements 16, 18, 20, and 22, and column 12, lines 7-11, of Roy et al. for support (final Office Action, page 5). Applicants respectfully disagree.

Initially, Applicants note that the Examiner also identified elements 16, 18, 20, and 22 as corresponding to the sprayer module. Applicants respectfully submit that it is unreasonable to allege that the same elements correspond to both the sprayer module that, among other things,

outputs a data packet on a selected channel and a plurality of preprocessing modules that, among other things, receives data packets from the sprayer module. Applicants noted this deficiency in the Examiner's rejection in a prior response. The Examiner maintained the rejection without commenting on Applicants' arguments. Applicants respectfully request that the Examiner explain, in detail, how elements 16, 18, 20, and 22 can be equated to both the sprayer module and the plurality of preprocessing modules, or withdraw the rejection.

Moreover, nowhere does Roy et al. disclose or suggest that elements 16, 18, 20, and 22 (which the Examiner alleged were equivalent to the plurality of preprocessing modules) receive data packets via a plurality of channels from elements 16, 18, 20, 22, 26, 52, 72, and 80 (which the Examiner alleged were equivalent to the sprayer module), as would be required by claim 17.

The Examiner also identified column 12, lines 7-11, of Roy et al. as allegedly disclosing the plurality of preprocessing modules (final Office Action, page 5). Applicants respectfully disagree.

At column 12, lines 7-11, Roy et al. discloses:

> The descriptor constructor 64 determines whether the data is an ATM cell or an IP packet and generates a corresponding interrupt to trigger the IPF/ATM look-up processor 66 to perform either IP routing look-up or ATM look-up.

Applicants note that this section of Roy et al. does not mention any of the elements identified by the Examiner as allegedly corresponding to the plurality of preprocessing elements or the sprayer module. This section also discloses nothing similar to a plurality of preprocessing modules for processing data packets, where each processing module receives data packets from one of the channels of the sprayer module, as required by claim 17.

Roy et al. also does not disclose or suggest a plurality of switching/forwarding modules, where each switching/forwarding module receives data packets from a corresponding one of the plurality of preprocessing modules, as further recited in claim 17. The Examiner alleged that Roy et al. discloses a plurality of switching/forwarding modules and identified Figure 2, column 6, lines 21-28, and column 23, claim 1, of Roy et al. for support (final Office Action, page 5). Applicants respectfully disagree.

Figure 2 of Roy et al. illustrates a switch element. Nowhere does Roy et al. disclose or suggest that any of the elements of Figure 2 receives data packets from a corresponding one of a plurality of preprocessing modules (which the Examiner alleged were equivalent to elements 16, 18, 20, and 22), as required by claim 17.

At column 6, lines 21-28, Roy et al. discloses:

> Turning now to FIG. 2, a switch element 100 according to the invention includes twelve "datapath and link bandwidth arbitration modules" 102 (shown only once in FIG. 2 for clarity). Each module 102 provides one link input 104 and one link output 106 through the switch element 100. Those skilled in the art will appreciate that data entering any link input can, depending on routing information, exit through any link output.

Nowhere does Roy et al. disclose or suggest that switch element 100 or module 102 receives data packets from a corresponding one of a plurality of preprocessing modules (which the Examiner alleged were equivalent to elements 16, 18, 20, and 22), as required by claim 17.

In claim 1, Roy et al. discloses:

> 1. A communications switch comprising:
>
> a) a plurality of port processors, each having at least one network interface; and
>
> b) a plurality of switch elements, each having a plurality of ports for coupling to said port processors, wherein
>
> each of said port processors has first and second switch element interfaces for coupling to one port of each of two switch elements, and

each of said port processors has automatic means for redirecting traffic to either of said first or second switch element interfaces in the event of switch congestion.

Nowhere does Roy et al. disclose or suggest that any of the elements of claim 1 receives data packets from a corresponding one of a plurality of preprocessing modules (which the Examiner alleged were equivalent to elements 16, 18, 20, and 22), as required by claim 17.

For at least the foregoing reasons, Applicants submit that claim 17 is not anticipated by Roy et al. Claims 19 and 22-24 depend from claim 17 and are, therefore, not anticipated by Roy et al. for at least the reasons given with regard to claim 17. Claims 19 and 22-24 also recite features similar to, but different in scope from, features recited in claims 1, 4-6, and 9-11. Claims 19 and 22-24 are, therefore, also not anticipated by Roy et al. for at least reasons similar to reasons given with regard to claims 1, 4-6, and 9-11.

REJECTION UNDER 35 U.S.C. § 103

In paragraph 4 of the Office Action, the Examiner rejected claims 2, 3, 8, 14, 20, 21, and 25-27 under 35 U.S.C. § 103(a) as allegedly unpatentable over Roy et al. in view of Ben-Zur et al. Applicants respectfully traverse the Examiner's rejection.

Claims 2, 3, 8, 14, 20, 21, 25, and 26 variously depend from claims 1, 12, and 17. Without acquiescing in the Examiner's rejection, Applicants submit that the disclosure of Ben-Zur et al. does not cure the deficiencies in the disclosure of Roy et al. identified above with regard to claims 1, 12, and 17. Therefore, claims 2, 3, 8, 14, 20, 21, 25, and 26 are patentable over Roy et al. and Ben-Zur et al., whether taken alone or in any reasonable combination, for at least the reasons given with regard to claims 1, 12, and 17. Claims 2, 3, 8, 14, 20, 21, 25, and 26 are further patentable over Roy et al. and Ben-Zur et al. for reasons of their own.

For example, claim 8 recites that the receiver module, the framer module, the sprayer module, the plurality of preprocessing modules, and the plurality of memories are mounted onto a single board. Neither Roy et al. nor Ben-Zur et al., whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 8.

The Examiner admitted that Roy et al. does not disclose the features of claim 8, but alleged that Ben-Zur et al. discloses these features and cited column 5, lines 18-21, of Ben-Zur et al. for support (final Office Action, page 7). Applicants respectfully disagree.

Ben-Zur et al. does not disclose or suggest anything similar to the receiver module, framer module, sprayer module, plurality of preprocessing modules, and/or plurality of memories recited in claim 8. Therefore, Ben-Zur et al. cannot disclose a receiver module, framer module, sprayer module, plurality of preprocessing modules, and plurality of memories mounted onto a single board, as required by claim 8.

In addition, at column 5, lines 18-21, Ben-Zur et al. discloses:

> The TMO switch of an embodiment is a data optimized SONET platform that integrates SONET ADMs, DCSs and ATM/FR switch functionality into a single platform using common card architecture.

Nowhere in this section does Ben-Zur et al. disclose a set of elements mounted onto a single board, let alone a receiver module, framer module, sprayer module, plurality of preprocessing modules, and plurality of memories mounted onto a single board, as required by claim 8.

Applicants identified this deficiency in the Examiner's rejection in a prior response. The Examiner maintained the rejection but did not address Applicants' arguments. If the Examiner maintains this rejection, Applicants respectfully request that the Examiner specifically identify

where Roy et al. or Ben-Zur et al. discloses or suggests the features of claim 8, or withdraw the rejection.

For at least these additional reasons, Applicants submit that claim 8 is patentable over Roy et al. and Ben-Zur et al., whether taken alone or in any reasonable combination.

Claim 14 recites features similar to, but different in scope from, features recited in claim 8. Claim 14 is, therefore, also patentable over Roy et al. and Ben-Zur et al., whether taken alone or in any reasonable combination, for at least reasons similar to reasons given with regard to claim 8.

Independent claim 27 is directed to a method of receiving data from a high-speed link. The method comprises receiving a stream of data signals at a data rate of at least approximately 10 Gigabits per second; deserializing the stream of data signals onto a multi-line bus; extracting data packets from the deserialized data; and spraying the data packets across a plurality of processing paths according to a load balancing or hashing technique.

Neither Roy et al. nor Ben-Zur et al., whether taken alone or in any reasonable combination, discloses or suggests the combination of features recited in claim 27. For example, neither Roy et al. nor Ben-Zur et al. discloses or suggests spraying data packets across a plurality of processing paths according to a load balancing or hashing technique.

The Examiner alleged that Roy et al. discloses this feature and cited column 3, lines 8-24, column 17, lines 11-17, column 23, claims 4 and 5, of Roy et al. for support (final Office Action, page 7). Applicants respectfully disagree.

At column 3, lines 7-24, Roy et al. discloses:

> A typical switch according to the invention includes multiple port processors and multiple switch elements. For a 48x48 "folded" switch, 48 port processors are coupled (four each)

> to 12 (first and third stage) switch elements and each of these twelve switch elements is coupled to 8 (second stage) switch elements. A three stage non-blocking switch according to the invention provides a total bandwidth of 240 Gbps and a five stage non-blocking switch provides a total bandwidth of 1 Tbps. An exemplary three stage folded Clos architecture switch includes forty-eight port processors and twenty switch elements. Four port processors are coupled to each of twelve (first and third stage) switch elements. Each of the twelve (first and third stage) switch elements are coupled to eight (second stage) switch elements. According to the presently preferred embodiment, each port processor is provided with means for coupling to two ports of a switch element or one port of two switch elements thereby providing redundancy in the event of a link failure.

Nowhere in this section, or elsewhere, does Roy et al. disclose or suggest spraying data packets across a plurality of processing paths according to a load balancing or hashing technique, as required by claim 27. In fact, Roy et al. does not even mention load balancing or hashing.

At column 17, lines 11-17, Roy et al. discloses:

> [Data stream deserializer 126] recovers the thirty-six-bit slot data from the row stream in a third FIFO which is used for deskewing the twelve input links. This deskewing allows all the input links to forward slot N to the switching core simultaneously. The link deskewing is controlled by the link synchronization and timing control module 150.

Nowhere in this section does Roy et al. disclose or suggest spraying data packets across a plurality of processing paths according to a load balancing or hashing technique, as required by claim 27.

In claims 4 and 5, Roy et al. discloses:

> 4. A communications switch comprising:
>
> a) a plurality of port processors, each having at least one network interface; and
>
> b) a plurality of switch elements, each having a plurality of ports for coupling to said port processors, wherein
>
> each of said port processors has first and second switch element interfaces for coupling to two ports of a single switch element, and
>
> each of said port processors has automatic means for redirecting traffic to either of said first or second switch element interfaces in the event of a switch failure or congestion.
>
> 5. A communications switch according to claim 4, wherein:

> each of said ports comprises two serial links which are interleaved to effectively double the bandwidth of a single serial link.

Nowhere in these claims does Roy et al. disclose or suggest spraying data packets across a plurality of processing paths according to a load balancing or hashing technique, as required by claim 27.

Ben-Zur et al. also does not disclose or suggest spraying data packets across a plurality of processing paths according to a load balancing or hashing technique, as required by claim 27.

For at least these reasons, Applicants submit that claim 27 is patentable over Roy et al. and Ben-Zur et al., whether taken alone or in any reasonable combination.

CONCLUSION

In view of the foregoing remarks, Applicants respectfully request the Examiner's reconsideration of the application and the timely allowance of pending claims 1-27.

If the Examiner believes that the application is not now in condition for allowance, Applicants respectfully request that the Examiner contact the undersigned to discuss any outstanding issues.

To the extent necessary, a petition for an extension of time under 35 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

By: _____
Paul A. Harrity
Reg. No. 39,574

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11240 Waples Mill Road
Suite 300
Fairfax, Virginia 22030
(571) 432-0800